



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

**APPLICANT:** Fitzgerald et al. **GROUP:** 2811  
**SERIAL NO:** 09/884,172 **EXAMINER:** Unknown  
**FILED:** June 19, 2001  
**FOR:** METHOD OF FABRICATING CMOS INVERTER AND  
INTEGRATED CIRCUITS UTILIZING STRAINED SILICON  
SURFACE CHANNEL MOSFETS

**Box Missing Parts**  
**Assistant Commissioner of Patents**  
**Washington, D.C. 20231**  
**Attn: Application Division**

**Sir:**

**COMPLETION OF FILING REQUIREMENTS**

In response to the Notice to File Missing Parts of Application mailed on August 16, 2001, a copy of which is enclosed, we enclose herewith the Declaration and Power of Attorney and a check for \$130.00 to cover the surcharge.

The Commissioner is authorized to charge Deposit Order Account No. 19-0079 for any further extension and/or fee that is required.

Respectfully submitted,

Matthew E. Connors  
Registration No. 33,298  
Samuels, Gauthier & Stevens LLP  
225 Franklin Street, Suite 3300  
Boston, Massachusetts 02110  
Telephone: (617) 426-9180  
Extension: 112

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231, Attn: Application Division.

  
Deborah M. Costello

Date

9/27/01